LAKSHMANAN BALASUBRAMANIAN

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Objective: To develop a professional expertise and build an outstanding career in the areas of high speed, low power digital and mixed signal VLSI with emphasis on wireless telecommunication and ambient intelligence applications.

Areas of interests: High speed and low noise CMOS VLSI design, signal integrity including substrate noise, mixed signal VLSI, DFT, communication systems engineering and DSP.

Professional experience:

1. ***Research Specialist,* jointly with IMEC vzw & ESAT-INSYS, KU,Leuven, Belgium.**
Sept 2001 – Present

Profile: Analysis and design techniques for reduced switching and substrate noise in mixed signal ICs and low power design.

Projects:

a. *Human++*, an ambient intelligence programme with wireless body area network. Presently designing high speed PFDs for low power PLLs in UMC 0.13µm, 1.2V CMOS technology.
b. Development of *SWAN*, a high level substrate noise analysis tool for technologies with high ohmic substrates. Developed a substrate macro model for high ohmic substrates. Designed a test chip in UMC 0.18µm, 1.8V CMOS technology, performed simulations and wafer probe measurements for substrate noise and substrate model characterization.

2. ***IC Design Engineer*, Texas Instruments India Ltd, India. Aug 2000 –Aug 2001**

Profile: Design For Testability for DSPs and broadband communication ICs.

Projects:

a. Developed the test specifications and test plan for *Puma*, a communications processor IC for Cable Modem applications and for *Taos*, a communications processor IC for wireless applications. Performed DFT and ATPG for *Drishti*, a real time DSP emulation system and for *Avalanche-D*, a data only version of the broadband communication processor IC.

Developed an integrated block level and chip level stuck and Iddq ATPG flow.

Academic qualifications:

1. ***Masters (M.Tech)* in Electronics Design and Technology, IISc, India. 1998-2000**

Distinction: CGPA 6.4/8, First class, GATE scholarship 1998-2000.

Thesis: "Active noise reduction in pilot's headset", sponsored by Defence Bioengineering and Electro medical Laboratory (DEBEL), India.

Other projects:

a. Implementation of a Digital PLL in an FPGA, 2000.
b. Design and implementation of a DC-DC converter (5V, 500A SMPS), 1999.
c. Design and Implementation of a high speed PN sequence generator in 1.2µm, 5V CMOS process using MAGIC layout editor, 1999.
d. Design and Implementation of a 29 bit DCO using PLDs (CY375I), 1998.

2. ***Bachelors (B.Tech)* in Electronics Engineering, Madras Institute of Technology, Anna University, India 1995-1998**

Distinction: CGPA 9.14/10, First class with Distinction, Rank 3 in University, 3/63 in the class.

Thesis: "Implementation of FPGA based GPS baseband processor", sponsored by Indian Space Research Organisation (ISRO).

Other projects:

a. AR modelling of speech process in Matlab, 1998.
b. Implementation of asynchronous event driven logic & micropipeline using FPGAs, 1997.
c. Keyboard & monitor interface using *ACTel FPGAs*, 1997.
d. Digital Oscilloscope with 10 x 10 LED matrix display, 1997.

e. Design and implementation of Digital Capacitance Meter, 1997.
f. Implementation of ECG simulator using 8031 microcontroller, 1996.
g. Digital Speech generation using SP0256AL2 and 8085, 1996.

3. ***Bachelors (B.Sc)* in Physics, University of Madras, India. 1992-1995**
Distinction: 81.82%, First class with Distinction, Rank 1/41.

Short courses and professional training:
1. Microwave techniques for microelectronics, Analog IC design, System Identification, FPGA based digital design technology and design of 10 channel digital radio.
2. Training on high-level verification of digital systems with Verisity's Specman Elite, Training on logic and gate level synthesis with Synopsys.
3. Workshops on Fundamentals of communication and Technical writing.

Publications:
1. M. Badaroglu, L. Balasubramanian, K.Tiri, V. Gravot, P. Wambacq, G. Van der Plas, S.Donnay, G. Gielen, H. De Man, "Digital circuit capacitance and switching analysis for ground bounce in ICs with high-ohmic substrates," in *IEEE Journal of Solid State Circuits - Special issue on European Solid-State Circuits Conference 2003, 2003. (Invited paper, yet to be published)*
2. M. Badaroglu, L. Balasubramanian, K.Tiri, V. Gravot, P. Wambacq, G. Van der Plas, S.Donnay, G. Gielen, H. De Man, "Digital circuit capacitance and switching analysis for ground bounce in ICs with high-ohmic substrates," in *Proceedings of the European Solid-State Circuits Conference 2003,* pp. 257-260, September 2003.
3. B. Lakshmanan, Sudarshan Dilip Solanki, Dr. M. K. Gunasekaran, Dr. G. Anandarao, Dr. P. P. Krishnapur, "Active noise reduction in pilot's headset" in *Journal of Indian Institute of Science*. (Submitted)

Professional affiliations:
1. **IEEE:** *Member* since 2002; Associate Member 2000 – 2002; Student Member 1998 – 2000.
2. **IEE:** *MIEE* since 2002; AMIEE 2000 – 2002; Student Member 1998 – 2000.
3. **Engineering Council of UK:***CEng* since 2000.

Language proficiency: English, introductory German, introductory Dutch, and Tamil.

Distinctions and awards:
1. Secured 93.37 percentile in Graduate Aptitude Test in Engineering (GATE), 1998 and awarded scholarship for pursuing M.Tech during 1998-2000.
2. Recipient of Rajam Ramaswamy Award for being the university topper in Control systems engineering, 1997.
3. Recipient of Top 1% in the state (Tamilnadu) award in National Graduate Physics Examination, 1995 conducted by Indian Association of Physics Teachers (IAPT).
4. Recipient of Top 10% in the centre award in the National Standard Physics Examination NSPE, 1992 conducted by Indian Association of Physics Teachers (IAPT).
5. Recipient of Tamilnadu Government Scholarship for outstanding NCC cadets, 1994.
6. Recipient of NCC National Cadet Welfare Society Scholarship, 1994.

Personal details: Unmarried, Indian national, born on 31 July 1975.