MINIMIZATION IN VARIATION OF OUTPUT CHARACTERISTICS OF A SOI MOS DUE TO SELF HEATING

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Abstract

The advantages of SOI MOSFETs over the bulk Silicon transistors are clouded by impact of self-heating on the output characteristics. An attempt has been made to minimize the variation in drain current by studying two different techniques. First, by providing a feedback path comprising Voltage & Current controlled sources. Another novel approach has been discussed which involves making changes in the values of some temperature dependent variables of the SOIMOS such that the variation in the Drain Current values due to effects of change in mobility & threshold voltage values in response to temperature increase neutralize each other.
Keywords*: SOI self heating, drain current minimization, controlled sources*

1.Introduction

The SOI MOS devices have substantial advantages over conventional MOS transistor structures such as high switching speeds, improved sub-threshold slope, reduced second order effects & elimination of latchup [1, 2]. The buried oxide layer acts as an insulating layer & is responsible for the heating up of the SOI MOS as the heat does not conduct through this layer readily. The increase in the temperature of the MOS is quite acute & can degrade the performance characteristics. Thus there is a need to try & minimize the variation in the drain current due to this self heating. Attempts have been made to try & make the SOI MOS work at almost constant output characteristics as the operating temperature increases. [3, 4, 5] If the self-heating effect of the SOI MOS can be negated, the other beneficial characteristics of the SOI technology can make it a potential substitute for applications requiring high speed switching characteristics.

2. Model Description – The FTGSOIMOS

Due to change in the operating temperature of the SOI MOSFET a change in some of the parameters of the MOS such as the mobility & the threshold voltage occurs. The quantitative change in the values of the surface ion mobility & the threshold voltage was calculated using the BSIM3v3SOI Model. It was noted that with the increase in the operating temperature of the MOSFET the mobility

degrades resulting in a decrease in the value of the drain current.

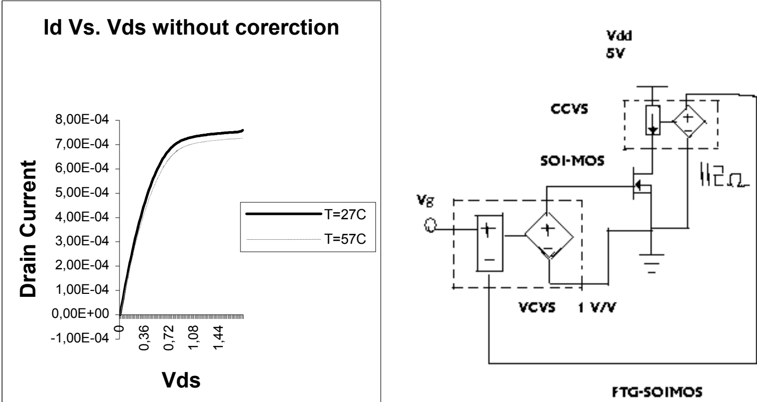

Fig 1. SOI Output characteristics at 27C & 57C. **Fig 2 FTGSOIMOS**

Fig 1. shows the temperature response of a SOI MOS with channel length = 1.0micron & width = 10micron at 27C and 57C. With an increase in operating temperature of 30 degrees over the room temperature it is seen that there is a decrease in the values of drain current by about 10% of its value at room temperature in the saturation region. An attempt to minimize this variation in the SOI drain current was made at the circuit level by providing a correcting feedback circuit as shown. The correcting **F**eedback **T**hermal **G**radient – **S**ilicon-**O**n-**I**nsulator **MOS** (FTG-SOIMOS) circuit shown in Fig2. consists of a feedback loop of two controlled sources. The current controlled voltage source (CCVS) provides a correcting voltage that is added to the gate terminal in accordance with the variation in the drain current values. The voltage controlled voltage source (VCVS) is used to add this correcting voltage to the gate voltage and has a gain of unity. The magnitude of the correcting voltage is adjusted by varying the transfer resistance of the CCVS such that the effect of decrease in the drain current is exactly compensated for by the increase in the gate bias. Simulation results in Fig3. show Id – Vds plot when the transfer resistance of the CCVS was kept at 112 ohm.

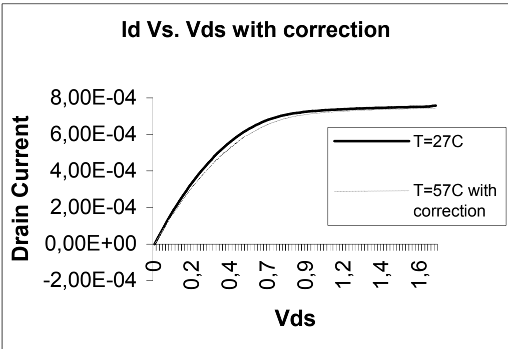

Fig 3. Output chars. of the FTGSOIMOS circuit

The variation in the drain current in the saturation region was reduced from 10% to less than 1%. The transfer resistance in this case is the determining parameter as by varying its value the gate bias can be varied & thus the drain current variation can be negated. The simulation results are obtained using Aimspice.

The basic feedback thermal model was discussed by Nooshabadi et al. [6] However, their model used two Voltage controlled sources as compared to one VCVS in the FTGSOIMOS. However the increase in area overhead acts as a deterrent to the application of this technique. An alternative solution was attempted by studying the Id - Vds characteristics for smaller device geometries at lesser values of gate-source bias. The device model equations for temperature variation reflected a phenomenon which if used put to use properly can help in minimizing the drain current variation without involving the area-overhead increase problem in the feedback model discussed here.

3. Device level study

At Gate – Source voltages less than about 1.0V for a short channel (0.25 micron or less) it is observed that the drain current does not decrease monotonically as the operating temperature of the SOI MOS increases. There is an increase in the drain current for a range of Vds values as the temperature increases and the Id-Vds plots at 27C and 57C cross each other once. The effect of self heating changes mainly two parameters viz. threshold voltage & mobility. Both the mobility & the threshold voltage decrease with temperature. The decrease in mobility tends to decrease the drain current while the decrease in threshold voltage tends to increase it. This behaviour is verified by simulation in Fig4.

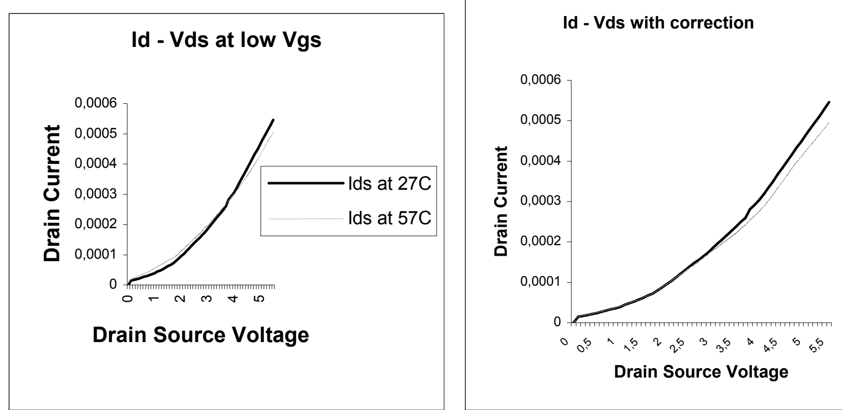

Fig4. Id – Vds characteristics at 27C & 57C at Vgs = 1.0V without correction (left) and with correction (right) in the values of temperature dependent parameters for threshold voltage and mobility

The BSIM3SOI model equation for the drain current is given below: [7]

$I_{ds,MOSFET} = \{I_{ds0}(1+ (V_{ds} - V_{dseff})/V_A) \} / (1 + R_{ds}I_{ds0}/V_{dseff})$

$\beta = \mu_{eff} C_{ox} W_{eff}/L_{eff}$

$I_{ds0} = \{\beta V_{gsteff}[1 - A_{bulk}V_{dseff}/2(V_{gsteff} + V_{th})]V_{dseff} \}/ (1 + V_{dseff}/E_{sat}L_{eff})$

The expressions for A_{bulk}, V_{dseff}, V_A, V_{gsteff}, R_{ds} etc. are given in [6].

The temperature response of the mobility & the Vth is given below:

$\mu_{0(T)} = \mu_{0(Tnom)} (T/T_{nom})^{\mu te}$

$V_{th(T)} = V_{th(Tnom)} + (T/T_{nom} - 1) * \{K_{T1} + (K_{tl1}/ L_{eff}) + K_{T2}V_{bseff}\}$

The temperature coefficients KT1, Ktl1, Kt2 & Ute have values dependent on the actual device characteristics such as doping, gate oxide thickness etc. &

values at room temperature are given in [7]. The values of these temperature dependent parameters can be made to vary within a certain range of values by varying the device characteristics. The range of values for KT1, Ktl1, Kt2 & Ute are given in [7]. It is seen that the effect of decreased mobility due to increased temperature on the drain current is to try & decrease the value of the drain current. Whereas the effect of decreased threshold voltage due to increased temperature is to cause an increase in the value of drain current. Thus we see that there are two countering effects acting on the drain current and we can obtain a device in which the voltage & current performance are relatively constant vis-à-vis temperature by suitably manipulating the values of for KT1, Ktl1, Kt2 which govern the response of threshold voltage to temperature & value of Ute which determines the amount of decrease in mobility for a given rise in temperature. An attempt at studying the possibility of such a device structure is made.

4. Results & Conclusion

The feedback correcting circuit of FTG-SOIMOS is one of the methods of minimizing the variation in the output characteristics of the SOIMOS. But it has limited hardware implantation capabilities due to the increased area overhead caused by the controlled sources. In the novel method discussed here by changing the temperature dependent parameter values we have tried to use the inherent characteristic of a MOSFET whereby the increase in temperature decreases the values of both ion mobility & threshold voltage but whereas decrease in mobility tends to decrease the drain current, the decrease in threshold voltage tends to increase the drain current. We have tried to balance these two effects by varying the values of KT1, Ktl1, Kt2 & Ute within a certain range so that the overall variation in the output characteristics is reduced considerably. However the exact nature of the dependence of each parameter on the device can be efficiently studied only by studying this effect on a device simulator which is currently unavailable with us.

5. References:

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