A QUANTITATIVE DRAIN CURRENT THERMAL MODEL FOR THERMAL GRADIENT CORRECTION IN A FULLY-DEPLETED SOI MOS

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1. Abstract

The localized heating of semiconductor devices on an integrated circuit can cause pronounced change in the operating characteristics of the circuit. This work proposes a mathematical model to calculate the changes in the output parameters of a FD SOI MOS used in the integrated circuits. The device characteristics change due to non-linearity in operation of the high heat dissipating MOS. The variation in the drain current of a MOS is plotted graphically & the mathematical model used to calculate this change shall be applied on a SOI MOS differential amplifier circuit. The graph with the applied correction for the change in the output current, as suggested by the mathematical model is also plotted for the SOI MOS and shall be applied on the differential amplifier in the final paper.

2. Introduction

Due to the low thermal conductivity of the back oxide, self-heating effects on SOI circuit performance are of major concern [1]. In the last few years SOI has been considered as a serious alternative for bulk CMOS for high performance and low power circuits [2, 3, 4]. The fully depleted (FD) SOI exhibits a very thin (<50nm) silicon layer, so that the depletion region extends through the entire layer [6]. They are of great interest due to potentially improved isolation. Enhanced inhibitions of the Short Channel Effects in SOI also contribute towards its favorability [7].

3. Significance of Thermal Behavior

The change in the drain current due to the change in the device parameters like Threshold Voltage and mobility has been modeled mathematically and plotted graphically with the correction applied to the drain current as suggested by the mathematical model. No such work has been reported for modeling of thermal gradients in the SOI domain using a quantitative model. A SOI MOS has been analyzed for simplicity. However, in the final paper the mathematical model shall be applied on the current sink MOS in a differential amplifier circuit. The model is generalized for any integrated circuit designed for low power applications using SOI CMOS logic.

The calculations have been done for operating temperature of 320K with 300K as the room temperature. The Gate-Source voltage has been taken as 1.7 Volt, the doping concentration in m^{-3} is given by Na = $1.6*10^{23}$. The mobility at 300 K is taken as $0.07 m^2/V-s$. The width – to – length ratio has been taken as 2.0.

A comparison between the output characteristics with & without the application of the mathematical correction has been shown. The mathematical correction can also be realized using some hardware & a few possible options for such hardware realization are discussed.

4. Variation with temperature of FD SOI parameters

4.1. Threshold Voltage

The effect of temperature is studied on the Threshold Voltage V_{TH} & the surface ion mobility μ. The FD SOI MOS device equations used are:

$$V_{TH} \cong \phi_{MS} + 2\phi_F - \frac{(Q_{OX} + Q_{DEPL})}{C_{OX}}$$

where ϕ_{MS}, ϕ_F, Q_{OX}, C_{OX}, Q_{DEPL} are the Metal-Semiconductor work function difference, the Fermi Potential, charge density in gate oxide, gate oxide capacitance and depletion charge controlled by gate respectively [10].

The gate oxide charge and the depletion charge do not vary much with temperature so they are neglected. The Fermi Potential is given by $\phi_F = kT/q \ln(\frac{Na}{n_i})$, [10] k is the Boltzmann constant, q is the electronic charge and Na is the doping concentration. Also,

$$\phi_{MS} = -\frac{E_G}{2} - \phi_F, \qquad \text{Thus} \qquad V_{TH} = -1/2\, E_G + \phi_F$$

Thus the equation for variation of the Threshold Voltage with the ambient temperature (T) becomes

$$\frac{\partial V_{TH}}{\partial T} = \frac{\partial \phi_F}{\partial T} - \frac{\partial E_G}{\partial T}$$

4.2 Mobility

We have the equation for mobility variation with temperature as

$$\mu_s(T) = \mu_{so}(T / To)^a$$

Where μ_{SO} is the electron surface mobility, T_0 is the room temperature (=300K) and 'a' is a process governed constant that varies between 1.5 and 2 which has been taken as 2.0 for the purpose of calculation [11].

4.3 Intrinsic carrier concentration

For the dependence of intrinsic carrier concentration in m^{-3} on temperature [14], we have

$$n_i = 3.9 \times 10^{16} T^{1.5} e^{-(EG/2kT)}$$

4.4 Band Gap Reference

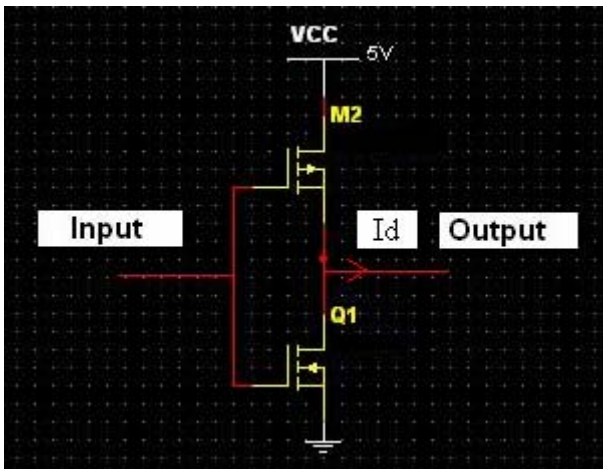
Temperature dependence equation for band gap reference gives [14],

$$E_G = 1.179 - 9.025 \times 10^{-5} T - 3.05 \times 10^{-7} T^2$$

SOI INVERTER

The circuit of a Fully Depleted SOI Inverter is considered for the thermal modeling consisting of a SOI pMOS and a SOI nMOS. The change in the output characteristics of the device is considered by modeling the change in the output current. Since the output current is the same as the drain current for either of the SOI MOS the change in the drain current I_D shall give the change in output characteristics. To keep the analysis simple the thermal effects of only the SOI nMOS are considered. The drain current [12] is given by

$$I_D = \tfrac{1}{2}\mu C_{OX}(\frac{W}{L})[V_{GS} - V_{TH}]^2 \quad \cdots\cdots\cdots(1)$$



A simple FD SOI MOS has been considered for the evaluation of the output characteristics

Taking up the device parameters of this MOS individually, we establish separate mathematical relations for the corresponding change in output circuit parameters

5. Mathematical Model

Taking the voltage drop across the SOI nMOS as V_{DS} the power dissipation in the device is $V_{DS} \times I_D$. This factor is responsible for the generation of heat in the device. This heat, in turn, raises the device temperature. Therefore the following heat balance equation holds

$$T - T_0 = mV_{DS} \times I_D$$

Here 'm' is a constant determined by the mass and specific heat of Si. Assuming that I_D is constant throughout the length of the device

$$\frac{\partial T}{\partial V_{DS}} = m \times I_D$$

5.1 Effect of V_{TH}

The variation of V_{TH} due to temperature [10] is $\frac{\partial V_{TH}}{\partial T} = \frac{\partial \phi_F}{\partial T} - \frac{\partial E_G}{\partial T}$

Or $$\frac{\partial V_{TH}}{\partial T} = 8.63 \times 10^{-5}[\ln(Na) - 38.2 - \frac{3}{2}(1 + \ln T)] + 9.025 \times 10^{-5}\,\mathrm{T} + 6.1 \times 10^{-7} \times \mathrm{T} \ldots\ldots\ (2)$$

From (1) the variation of drain current with threshold voltage is,

$$\frac{\partial I_D}{\partial V_{TH}} = -\mu C_{OX}(\frac{W}{L})[V_{GS} - V_{TH}]$$

The overall equation for I_D variation with V_{DS} due to the thermal gradient is

$$\frac{\partial I_{D(V_{TH})}}{\partial V_{DS}} = \frac{\partial I_D}{\partial V_{TH}} \times \frac{\partial V_{TH}}{\partial T} \times \frac{\partial T}{\partial V_{DS}}$$

$$= -\mu C_{OX}(\frac{W}{L})[V_{GS} - V_{TH}] \times [9.025 \times 10^{-5} + 6.1 \times 10^{-7}\ \mathrm{T} + 8.63 \times 10^{-5}$$

$$\times [\ln(Na) - 38.2 - \frac{3}{2}(1 + \ln T)]\ ] \times mI_D \quad (2.1)$$

5.2 Effect of mobility

The variation of mobility [11] with temperature is

$$\frac{\partial \mu}{\partial T} = \frac{a}{T_O} \times \mu_{SO} \times (T / T_O)^{\text{a-1}} \cdots\cdots (3)$$

From (1) the variation of drain current with mobility is given by,

$$\frac{\partial I_D}{\partial \mu} = \tfrac{1}{2} C_{OX}(\frac{W}{L})[V_{GS} - V_{TH}]^2$$

The overall equation for I_D variation with μ due to the thermal gradient is,

$$\frac{\partial I_{D(\mu)}}{\partial V_{DS}} = \frac{\partial I_D}{\partial \mu} \times \frac{\partial \mu}{\partial T} \times \frac{\partial T}{\partial V_{DS}}$$

$$= \tfrac{1}{2} C_{OX}(\frac{W}{L})[V_{GS} - V_{TH}]^2 \times \frac{a}{T_0} \mu_{SO}(\frac{T}{T_0})^{\text{a-1}} \times mI_D \quad (3.1)$$

6. Results & Discussion

The total change in the output current due to the thermal gradient across the SOI nMOS is given by the sum of the small changes contributed by the various parameters of the device being analyzed. $\frac{\partial I_D}{\partial V_{DS}} = [\frac{\partial I_{D(VTH)}}{\partial V_{DS}} + \frac{\partial I_{D(\mu)}}{\partial V_{DS}}]$

The total change given on the right hand side of the above equation when multiplied by the differential voltage drop across the drain source terminal of the SOI nMOS would give the total change in the output circuit current due to heating of this device in excess of its normal operating value. This value of the change in output current is adjusted in the drain current equation & the result is shown graphically with this mathematical correction.

The % reduction in the variation of the Drain Current Id on the application of the mathematical correction is 3.03% as compared to a variation of 14.91% without the correction. Further accuracy can be achieved if we consider the variation in the intrinsic carrier concentration & the Energy Band Gap reference as well.

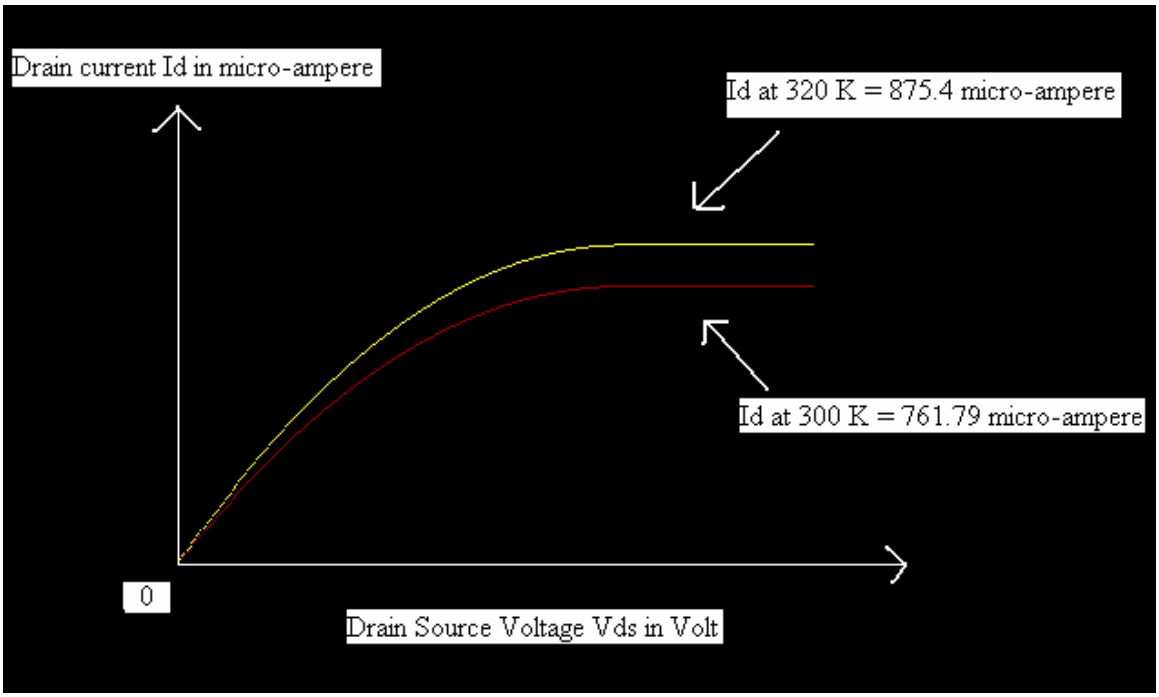
7. Hardware Realization

The predicted improvement in the device output characteristics by the application of the mathematical model discussed above can be implemented on some IC. One of the basic circuits is the one used in [15] where Current & Voltage controlled sources have been used to monitor the variation in the current characteristics. However the closed loop feedback network considered here suffers from the drawback of large area overhead. As

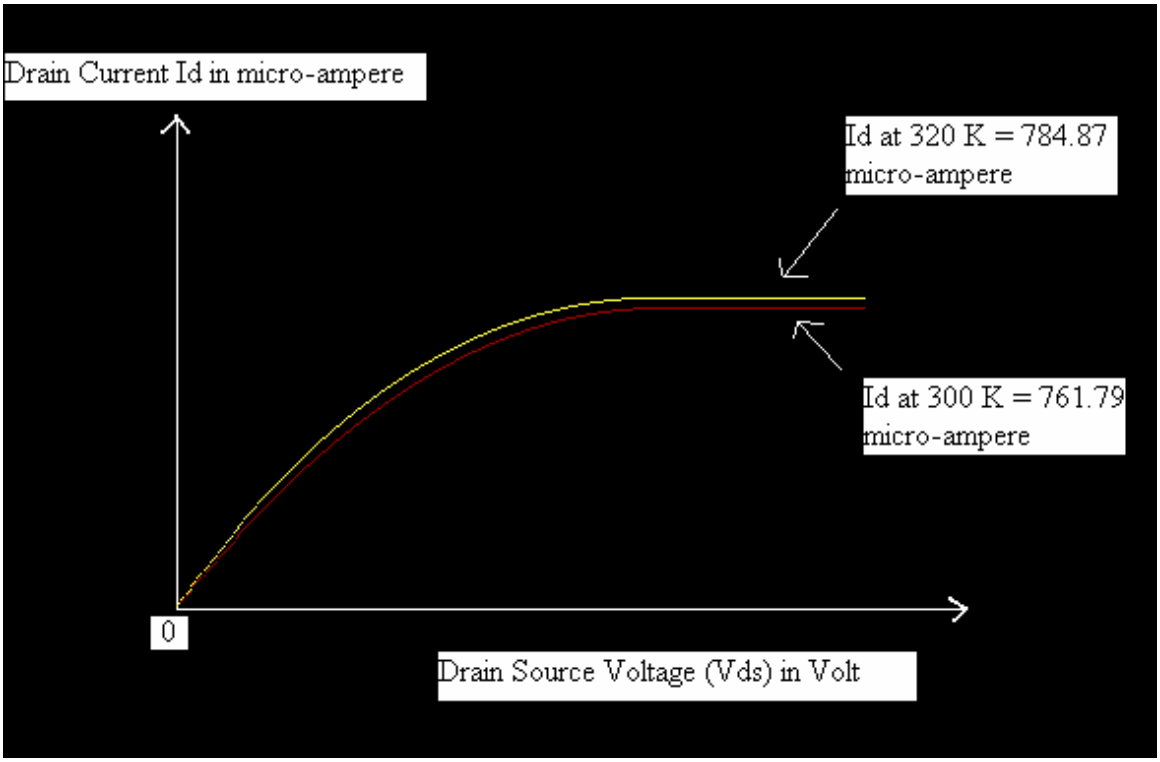
such it is not practically feasible. Some of the other possible options are to connect a MOS resistance across the device so that the change in the drain current as given by this mathematical model is compensated by the MOS resistance that is added. Such a network would be practically realizable but the work could not be carried forward due to the lack of a SOI simulation tool. The present graphs involve a simple C program to simulate the variation in the output parameters.

8. Conclusion

An efficient mathematical model for SOI MOS thermal behavior has been proposed. More enhanced modeling can help a long way in predicting the device characteristics even in the presence of thermal gradients and in the case of high power dissipating devices a major portion of the power consumed due to such localized heating can be accounted for to obtain more accurate estimation of the actual performance of the circuit.



The output characteristics of the MOS inverter – Id Vs Vds – without the application of the mathematical correction. The values of Id are calculated at 300 K & 320 K.



The output characteristics show a marked improvement on the inclusion of the correcting term for the drain current Id. The characteristics can be improved by the inclusion of the effect of thermal gradient on the intrinsic carrier concentration & the Energy Band Gap reference.

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