<u>Address:</u> No.10, Sriram Colony, Tambaram Sanatorium, Chennai, India. Zip: 600047

Arvind Raj Mahankali Sridhar

Objective	A research career in Electromagnetics and its applications in VLSI.
Education	Bachelor of Engineering in Electronics and Communication Engineering (2002–2006)
	College of Engineering Guindy, Anna Univesity, Chennai CGPA (upto sixth semester): 8.813/10
Skills	Software Skills
	Experience with VHDL, C, Assembly Languages (8085, 8086, 8051) and MATLAB programming.
	Electronics Tools
	Experience with TMS320c5X processor emulator, Emulator 8086, RIDE microcontroller simulator, FPGA ADV, Modelsim, Leonardo Spectrum, Synplify, Actel Designer, Silicon Sculptor, EMpire Electromagnetic Simulator.
	Hardware Exposure
	Rich experience in Actel and Cyclone FPGA designs from simulation through fusing and testing, 80186 processor and 89S8252 microcontroller
Projects	Interconnect Delay Optimization in High Speed VLSI circuits (Ongoing)
	I'm currently working on a project titled "Modeling and Optimization of Interconnect and Packaging for High Throughput On-Chip and Off-Chip Communications" mentored by Dr. Arun Chandrasekar of Intel India (Semiconductor and Packaging division). This project attempts to find modeling and optimization techniques of interconnect and packaging for better performance in High Speed VLSI circuits. This project has been presented as poster at the Intel India Student Research Contest 2005.
	IC Design of Passive Power Transfer and BPSK Communication for
	Implanted Devices (On going) My final year project deals with the ASIC design for passive power transfer (using inductive coupling) and BPSK communication link to be used in implanted device. This project is expected to go till the Lay Out stage. The main design issues in this project is the Low Drop Out Voltage Regulator, Band Gap Reference, DC-DC Step up converter and a Start-Up circuit for the power transfer part and VCO, Comparator and Chopper Multiplier for the BPSK part.
	Developing General Purpose Genomic Signal Processor (Ongoing) I'm currently involved in developing a general purpose Genomic Signal Processor. This processor-implemented in an Altera NIOS Soft Core processor on an Altera Cyclone FPGA platform- uses Hidden Markov Model to identify coding regions in a given genetic sequence and also finds common functionalities in protein sequences.

Military Standard 1553 protocol for communication between payloads in the Statellite

I have implemented a communication protocol (Mil. Std. 1553) between the Bus Electronics board and Payload boards which are a part of the ANUSAT- the Micro Satellite being developed by Anna University in collaboration with ISRO.

Navigational Solutions in the GPS Receiver in ANUSAT

I have implemented the Navigational Solutions- from Ephemeris data synchronization to the Position Fix- for the GPS receiver to be implanted in the ANUSAT in 80186 Microprocessor.

UART interface between FPGA and Computer System

I have implemented an UART controlling interface between FPGA and Computer System via an 8086 Microprocessor which is being used for real-time payload testing for the ANUSAT Micro Satellite

S and F Receiver for ANUSAT

I'm involved in the process of validating the Store and Forward Receiver board to be put up in ANUSAT. This consists of testing the RF ADC.

Automatic Navigation System

I have developed an 8051 Microcontroller-based Automatic Navigation System where in an automobile navigates itself through a Matrix of roads through the shortest path. This project was presented at Pragyan- the National level technical symposium of NIT, Trichy

Bit-Jet

This is the implementation of Frequency Division Multiplexing in FSK communication realized using multiple FSK generators and PLL and analog adder. This project won the Second Prize in Techshow 2004- the intra college Technical Symposium organized by Computer Society

Iris Pattern Recognition

This is a software implementation of recognition of a person's identity using his/her Iris pattern by using Fourier Miller Transform.

Research Research experience at the Integrated Systems Laboratory, Department of ECE, College of Engineering Guindy. Lab Website: http://www.annauniv.edu/dece/isl/index.htm

 GRE
 Verbal: 590/800
 Quantitative: 800 / 800
 Analytical Writing: 5.5 / 6

 Toefl
 Listening: 30/30
 Structure/Writing: 30/30
 Reading: 30/30
 Essay: 6/6

 Interests
 Physics, in particular, Electromagnetics. VLSI design.