2.44-Ghz LNA for Bluetooth™ Transceiver

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Abstract **-** A low power and linear 2.45 GHz low-noise amplifier was designed using 0.18µm CMOS technology. Input and Output matching network was implemented with on chip Inductors to minimize This LNA design has been simulated with Spectre-RF and the results shows that it provides a gain of more than 22dB, for a noise figure of 0.84dB, and an input referred IP3 of +7.39 dB while consuming only 3.324mA current.

Index – LNA, RFIC, Bluetooth

1. Introduction

Until recently, radio frequency integrated circuits (RFIC's) were implemented in GaAs and SiGe technologies because of their relatively high unity gain cutoff frequency f_T. But due to recent advances in CMOS technology, the minimum feature size of CMOS device is decreasing and as a result the f_T of the transistors continues to improve and has reached to a point where f_T of CMOS is comparable to those in GaAs and SiGe processes. With deep sub-micron CMOS device, f_T exceeding 100Ghz and minimum noise figure less than 0.5 dB could be achieved. Due to these good RF characteristics and other advantages like low cost and possibility of integrating RF, IF and Baseband blocks of transceiver on single substrate, CMOS is becoming most preferred technology for new wireless communications applications like Wireless LAN, Bluetooth, etc.

LNAs are usually placed at the front-end of a receiver system, immediately following the antenna. A band pass filter may be required in front of it but this filter generally degrades the noise performance of the system. The purpose of an LNA is to boost the desired signal power while adding as little noise and distortion as possible so that retrieval of this signal is possible in the later stages in the system

Research in recent years on CMOS LNA design has investigated various features like topology, improvement of low noise figure, high power gain, and high linearity. All these features were considered by us in our LNA design and we tried to achieve the specifications shown in table I.

Table I
Characteristics and Specifications of an LNA

Characteristic	Specification
Noise Figure	NF < 3 dB
Gain	A_v > 15 dB
Centre frequency	*f =2.45 GHz*
Other characteristics	2:5V Power supply 0.18µm process Fully differential 50 input impedance

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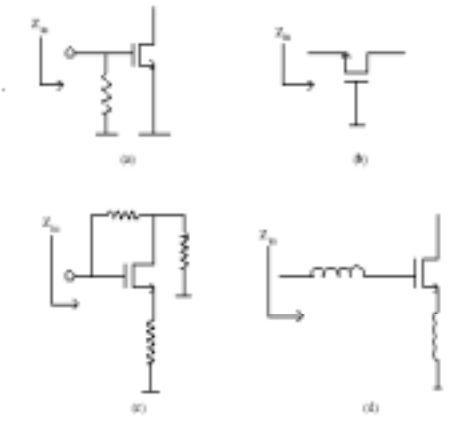

Fig 1: Common LNA architectures. (a) Resistive termination, (b) 1/gm termination, (c) shunt-series feedback, (d) inductive degeneration

2. Theory

There are several common objectives to be met in the design of CMOS low noise amplifiers. They are minimizing the noise figure of the amplifier, providing gain with sufficient linearity and providing a stable 50Ω input impedance.

We now examine, in detail, the requirement of providing stable input impedance. To present known resistive impedance to the external world, a number of circuit topologies as shown in figure 1 were examined and we then narrowed the field of contenders.

The MOSFET input impedance is inherently capacitive, so providing a good match to a 50 resistance without degrading noise performance would appear to be difficult. Simply putting a 50 resistor across the input terminals of a common source amplifier as shown in figure 1(a) adds thermal noise while attenuating the signal ahead of the transistor. This produces unacceptably high noise figures. Another method as shown in figure 1(b) for realizing a resistive input impedance is to use a common-gate configuration since the resistance looking into the source terminal is 1/gm a proper selection of device size and bias current can provide the desired 50 resistance. But the noise figure of this configuration would be high for high frequencies due to the gate current noise of the transistor. The third configuration (figure 1(c)) uses a resistive shunt and series feedback to set the input and output impedances of the LNA. But this has high power dissipation compared to others with similar noise performance due to the fact that shunt-series amplifiers of this type are naturally broadband, and hence techniques which reduce power consumption through LC tuning are not applicable. It also requires on-chip resistors of reasonable quality, which are generally not available in CMOS technologies. We found that the fourth architecture shown in figure 1(d), employing inductive source degeneration, is the best method. With such an inductance, a real term in the input impedance can be generated without the need of real resistances which degrade the noise performance. Tuning of the amplifier input then becomes necessary, making this a narrow band approach which is favorable for our application.

The design procedure followed for our LNA design has been taken from [3] which suggests a 3 step approach. First, use eqn [1] to determine the necessary device width such that the noise figure would be minimized. Then bias the device with the amount of current allowed by power constraint. Next, select the value of source degenerating inductance to provide the necessary input match, using the value of ω_T that corresponds to the bias conditions.

$$W = \frac{1}{3\omega LCoxRs} \qquad \ldots(1)$$

In the next few lines, we describe how above three steps lead to an input matching. For simplicity, we consider a device model (Fig 2) that includes only a transconductance

$$Z_{in} = jw(L_g + L_s) + (1/jwC_{gs}) + (g_m L_g / C_{gs})$$

and a gate-source capacitance, it can be seen that the input impedance of the circuit is

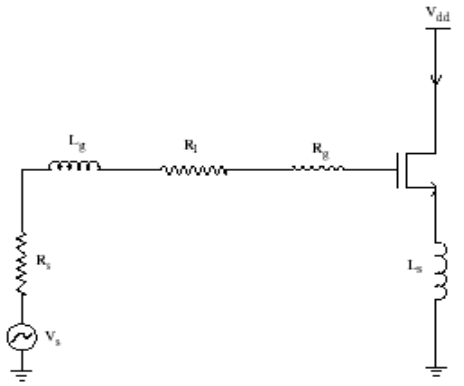

Fig. 2. Equivalent circuit for the input stage

As can be seen, the input impedance is that of a series RLC network, with a resistive term that is directly proportional to the inductance value.

The gate inductance L_g and ω_T were obtained in the 3 step process described earlier. What remains is L_s, which can be easily calculated setting the magnitude of the real term i.e. $\omega_T L_s$ equal to 50. This completes the input matching.

3. Simulation Results

We simulated our LNA design using Spectre-RF (a RF spice simulator of Cadence).

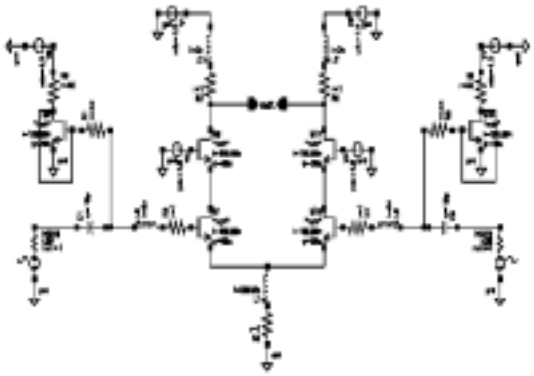

Fig 3: LNA Schematic

We extracted the S-parameters of our LNA and did S-parameter analysis to measure the stability, gain, VSWR and Noise figure of it. We also did PSS (Periodic Steady State) Analysis to measure the linearity (IP3) of our LNA design.

We now present the results of the simulation of the circuit and compare the performance to the given specifications.

A. Input Matching

The first constraint on the LNA was to assure that the input impedance matches the source impedance, i.e. the LNA presents a purely resistive load of 50 to the antenna, in order to maximize the power transfer. In order to verify this, we simply plot the input and the output VSWRs as shown on Fig 4 . For input, we obtained a VSWR of 1.47 and an output VSWR of 1.51 was achieved.

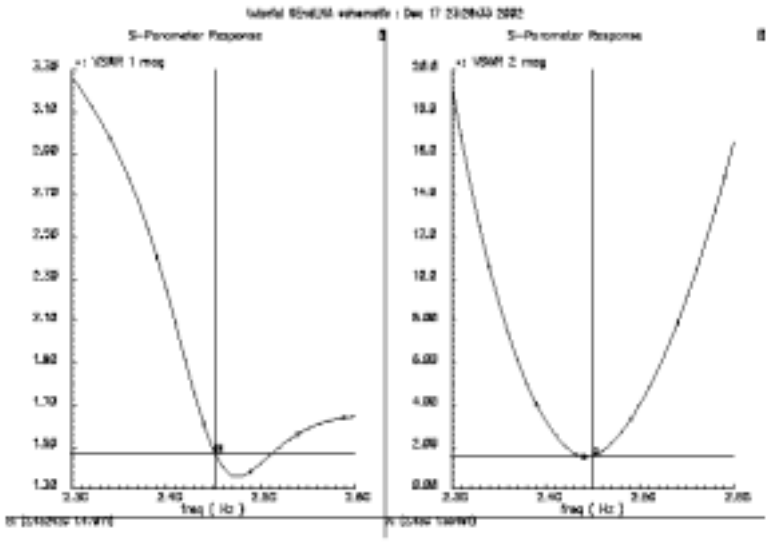

Fig 4: Input (left plot) and Output (right plot)VSWR as a function of frequency

B. Gain

The following plot (Fig 5) shows the gain as a function a frequency. We obtained a gain of 22.64 dB.

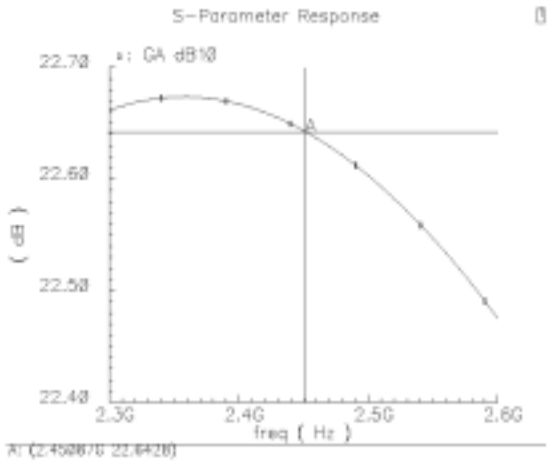

Fig 5 : Plot of available as function of frequency

C. Noise Performance

As shown in Fig 6, S_{11}* is close to Γ_{opt} and as such the noise figure obtained is small. We obtained a noise figure of 0.842 dB for an operating frequency of 2.45 GHz.

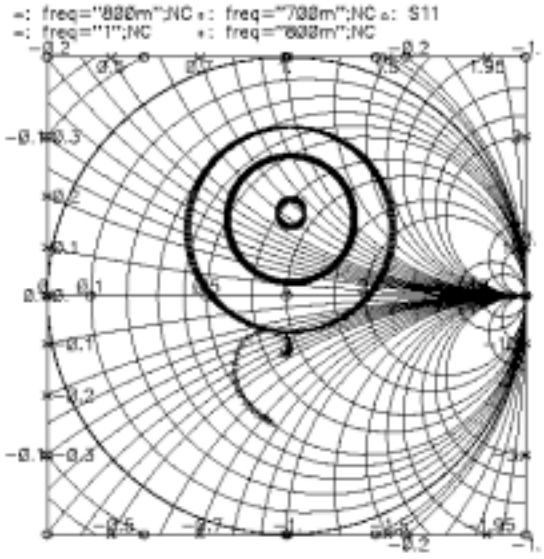

Fig 6 : Smith Chart plot of S11 and noise circles

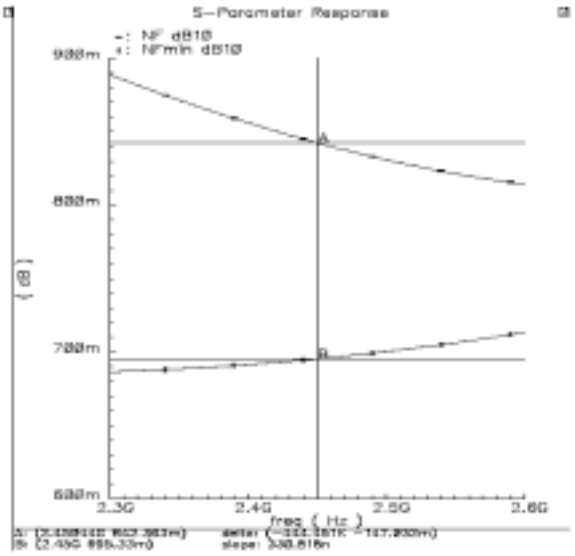

Fig 7 : Plot of NF and NF_{min}

D. Linearity

A two-tone technique was used to measure IP_3 with the frequencies being f_1= *2.4 GHz and* f_2*= 2.41 GHz.* And an IP_3 of 7.34 dBm was obtained.

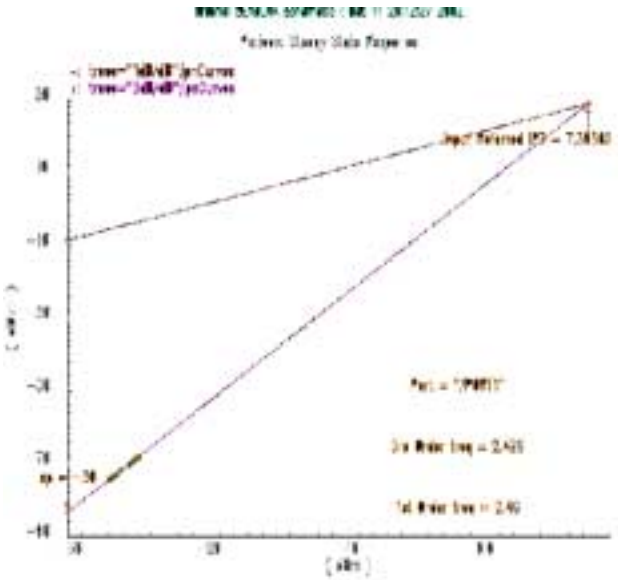

Fig 8: Input referred IP_3 of LNA

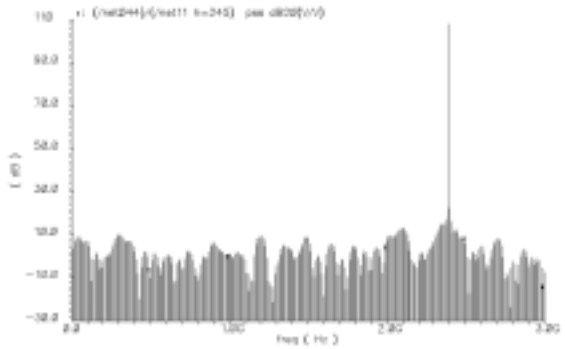

Fig 9: Output voltage distribution

4. Conclusion

We have designed a low noise amplifier for a Bluetooth Transceiver in a 0.18μm CMOS process. We met all the specifications given to us. The following table summarizes our LNA design.

Frequency	2.45 Ghz
Ga (Gain)	22.64 dB
Mag(S21)	22.67 dB
NF50 (Noise Figure)	0.842 dB
NFmin (dB)	0.695 dB
IP3	+7.39 dB
Input VSWR	1.47
Output VSWR	1.51
Supply Voltage	1.5 Volts
Current Dissipation	3.324mA

5. References

[1] Bosco Leung, *VLSI for Wireless Communication*, Prentice Hall Electronics and VLSI Series, 2002

[2] Guillermo Gonzalez, *Microwave Transistor Amplifiers*, 2nd edition, Prentice Hall, 1997.

[3] Thomas Lee, *Design of CMOS RF IC*, Cambride University Press, 2001

[4] Behzad Razavi, *RF Microelectronics*, Prentice Hall 1998