

# Brief Papers

## A 15-b Pipelined CMOS Floating-Point A/D Converter

Dwight U. Thompson and Bruce A. Wooley, *Fellow, IEEE*

**Abstract**—A floating-point approach can be used to extend the dynamic range of analog-to-digital (A/D) converters in applications where large signals need not be encoded with a precision greater than that required for small signals. Owing to the nonuniform nature of the quantization in a floating-point A/D converter (FADC), it is possible to sacrifice a large peak signal-to-noise ratio to obtain savings in power dissipation and area while achieving a large dynamic range.

A 15-b switched-capacitor pipelined FADC has been designed with a 10-b mantissa and an exponent that provides an additional 5 bits of dynamic range. The increased dynamic range is obtained with a three-stage pipelined variable gain amplifier, while the mantissa is determined by a uniform 10-b pipelined A/D converter. An experimental prototype of the converter has been integrated in a 0.5- $\mu\text{m}$  CMOS technology. It achieves a dynamic range of 90 dB at a conversion rate of 20 MSamples/s with a total power dissipation of 380 mW.

**Index Terms**—Analog-digital conversion, CMOS analog integrated circuits, floating-point A/D conversion, mixed analog-digital integrated circuits, switched-capacitor circuits.

### I. INTRODUCTION

IN RECENT years, pipelined switched-capacitor topologies have emerged as an especially attractive approach to implementing power-efficient Nyquist-rate A/D converters with medium-to-high resolution at medium-to-high conversion rates [1], [2]. In addition, floating-point A/D converters (FADCs) have been shown to be a useful means of providing a large dynamic range in applications where large signals need not be encoded with a precision greater than that needed for small signals. Floating-point analog-to-digital converters have historically found use in the instrumentation of experiments in which the acquired signal is of a nonrepeatable nature, such as those resulting from explosions, impacts, or earthquakes. Specifically, they have been used for large dynamic range data acquisition in high-energy physics instrumentation, such as electromagnetic calorimeters for detectors in colliding-beam machines [3]–[5]. Converters with nonuniform quantization may also be attractive in some communications applications in which low-amplitude signals must be acquired and processed with a signal-to-noise ratio (SNR) in the range of 40 to 70 dB. Owing to the nonuniform nature of the quantization in a floating-point converter, it appears possible to sacrifice a large

peak SNR to obtain savings in power dissipation and area while achieving a large dynamic range. The objective of this work is to combine the techniques of Nyquist-rate pipelining and floating-point conversion to achieve a significant increase in dynamic range without stringent linearity requirements or the overhead of complex calibration logic.

Floating point architectures can be used to extend the dynamic range of Nyquist-rate A/D converters beyond ten bits without the need for calibration. In such architectures, the dynamic range can be much larger than the resolution with which large signals are quantized. The peak SNR is then governed by either the circuit imperfections or, if the large signal resolution required is only ten bits or less, system considerations. The linearity required in the circuits used to implement the converter, which is governed by component matching, operational amplifier (opamp) performance, settling time, capacitor linearity, and the sample-and-hold network, is also relaxed.

The architecture described in this paper comprises a three-stage switched-capacitor variable gain amplifier (VGA) followed by a uniformly quantized pipelined ADC with digital error correction. No calibration is needed to achieve a peak signal-to-noise-plus-distortion ratio (SNDR) of approximately 60 dB. A 15-b switched-capacitor pipelined FADC has been designed with a 10-b mantissa and an additional five bits of dynamic range. The extra dynamic range is obtained with a three-stage pipelined VGA, while the mantissa is determined by a subsequent 10-b uniform pipelined A/D converter. An experimental prototype of the converter has been implemented in a 0.5- $\mu\text{m}$  CMOS technology. This converter achieves a dynamic range of 15 bits at a conversion rate of 20 MSamples/s with a total power dissipation of 380 mW.

### II. FADC QUANTIZATION

Unlike uniform A/D converters, which for a specified conversion rate, power dissipation, and dynamic range can often serve a myriad of applications, nonuniform converters are generally designed with only a specific application in mind, usually with unique system requirements. A nonuniform A/D converter can be designed to meet the requirements of systems demanding a large dynamic range with minimum area and complexity, while allowing for relatively high nonlinearity. A number of different approaches to nonuniform A/D conversion have been proposed and demonstrated.

Floating-point A/D conversion typically employs two basic operations in addition to uniform quantization. First, the level, or range, of the magnitude of the input signal is detected and

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The authors are with the Center for Integrated Systems, Stanford University, Stanford, CA 94305-4070 USA (e-mail: duthomp@par.Stanford.edu).

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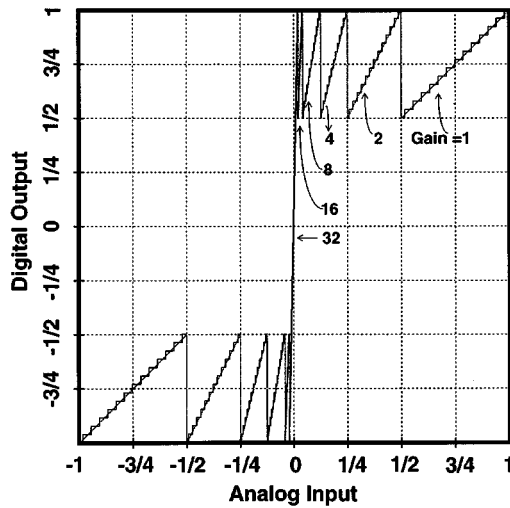
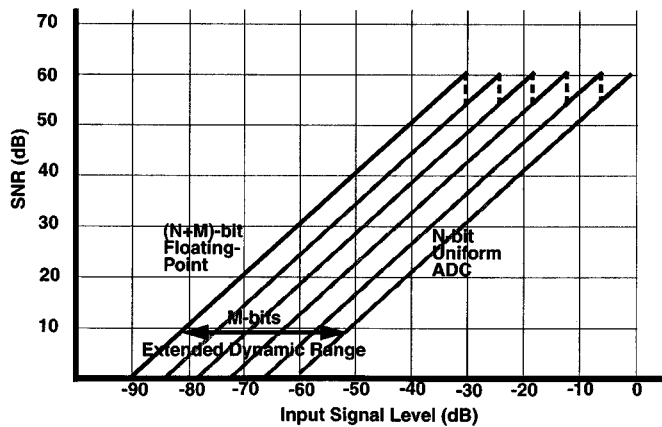


Fig. 1. FADC transfer characteristic.

Fig. 2. Signal-to-quantizing noise ratio versus input signal level for an FADC with  $N$  bits of quantization and  $M$  bits of extended dynamic range.

encoded as an exponent. Then, the signal is scaled according to the value of the exponent and prior to the quantization that determines the mantissa. Typically the signal scaling is by powers of 2. If the scaling extends the dynamic range by  $M$  bits, the dynamic range for an FADC with an  $N$ -bit mantissa is  $M + N$  bits. The number of bits of extended dynamic range,  $M$ , can be encoded in an exponent of  $x$  bits, where  $x$  is the minimum integer greater than or equal to  $\log_2(M + 1)$ .

Fig. 1 shows an example of the voltage-transfer characteristic for an FADC in which the input signal is scaled, or amplified, prior to uniform quantization. As the level of the input signal decreases, the signal range is amplified so as to reach the full scale of the subsequent uniform quantizer. In Fig. 1, the gain values are 1, 2, 4, 8, 16, and 32. As the input signal magnitude decreases by a factor of 2, the quantization step size, and thus the quantization error, is correspondingly reduced by a factor of 2. In this example, the dynamic range is extended by  $M = 5$  bits, and the magnitude of the signal is partitioned into  $M + 1 = 6$  binary-weighted gain segments.

Fig. 2 shows a plot of signal-to-quantization-noise ratio (SNR) versus input signal for a 15-b FADC with a 10-b mantissa and an exponent providing an extra five bits of dynamic

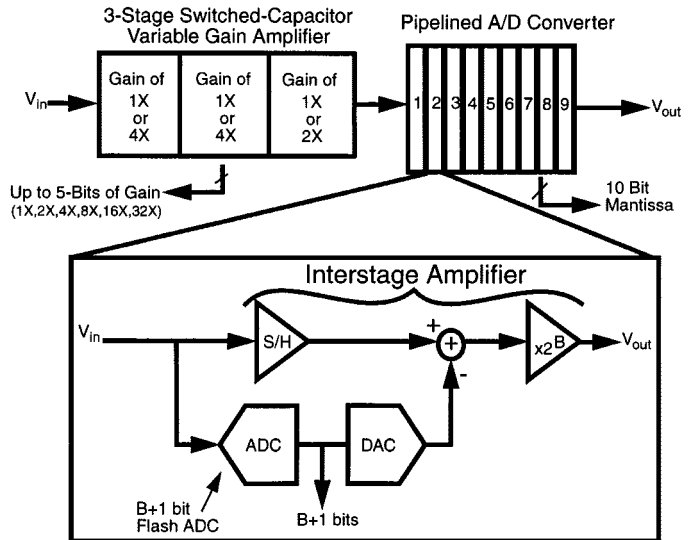


Fig. 3. Overview of FADC with three-stage VGA, followed by a uniform pipelined A/D converter.

range. The overall FADC SNR is a composite of the SNRs of each of the  $M + 1$  number of uniformly quantized gain segments. As the input signal level increases from the minimum detectable input level, the SNR increases linearly as it would for a uniformly quantized ADC. However, once the input level increases past the last step in the smallest input gain segment, the quantization step size doubles, and the FADC SNR shifts to trace along the uniformly quantized SNR curve for the larger step size. The maximum SNR is limited by the resolution of the FADC, i.e., the number of uniformly quantized bits in the mantissa.

FADC implementations can be classified into several categories: charge integration FADCs, cyclic or algorithmic FADCs, and FADCs employing a VGA followed by a uniform A/D converter. In the FADC architecture with a VGA, low-level inputs are amplified prior to quantization with a uniform quantizer [5]. The uniform A/D converter usually consists of a medium-to-high speed Nyquist-rate converter, such as a flash, two-step, folding, or pipeline architecture [6]. Hence, FADCs typically provide a maximum conversion rate comparable to those of uniformly quantized Nyquist-rate converters. However, the nonuniform architecture can reduce the complexity, signal processing, die area, linearity, and calibration requirements when compared to similar uniform Nyquist-rate architectures.

### III. PIPELINED FADC IMPLEMENTATION

The architecture of the proposed converter is illustrated in Fig. 3. In this converter, a three-stage switched-capacitor VGA is used to amplify low-level signals into the input range of the subsequent uniformly quantized pipelined A/D converter. Large-amplitude signals pass directly to the pipeline A/D converter input. The VGA can amplify the input signal, by factors of 2, up to a maximum of  $M$  bits before the uniformly quantized A/D converter quantizes the signal to  $N$  bits. The gain of the VGA is determined by comparing the input signal to a set of reference levels using on-chip comparators.

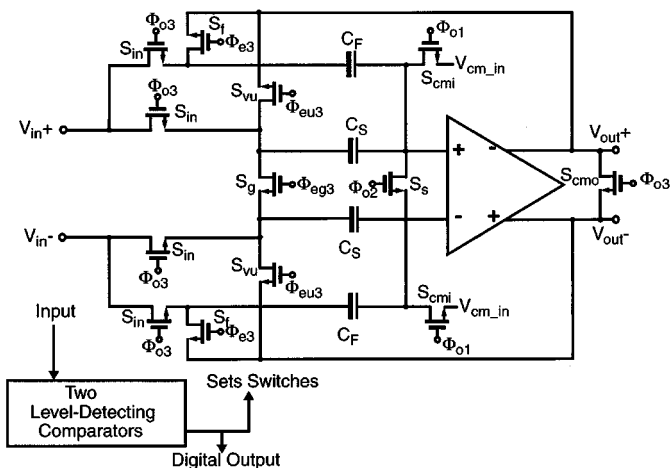


Fig. 4. Schematic of a VGA stage.

### A. Variable Gain Amplifier

The pipelined VGA architecture is an appropriate approach when the overall system requirements can tolerate the latency through the VGA stages. The pipeline VGA stage, as shown in Fig. 4, has an architecture similar to a stage in the pipelined ADC; hence, its design, clocking, data amplification rate, and layout are similar to those of the ADC stage.

The number of stages in the pipeline VGA depends on the number of possible gain settings for the system. Each low-gain switched-capacitor gain stage amplifies the input signal by a closed-loop gain  $G_i$ , and the total gain  $G_{\text{Total}}$  is

$$G_{\text{Total}} = G_1 G_2 \dots G_K = \prod_{i=1}^K G_i \quad (1)$$

for  $K$  stages.

The gain of each VGA stage is adjusted depending on the total gain required to amplify the signal to the input range of the uniform ADC. As indicated in Fig. 3, in the first two stages of the VGA the gain may be set to either unity or four, while the third-stage gain is either unity or two. The larger gains are used in the first two stages in order to minimize the sensitivity to noise in subsequent stages of the pipeline for small signals. The gain of the VGA, and thus the input signal range, is determined by using two high-speed low-offset comparators in each VGA stage to detect the signal level.

The data latched into the two low-offset comparators that are used to detect the signal level at the input of the VGA stage determine the gain of the stage during the amplify/hold phase. For input voltages above the “positive” amplitude threshold or below the “negative” amplitude threshold, switches  $S_f$  and  $S_{vu}$  both conduct, and the gain of the stage is unity. For input levels between the two comparator thresholds, the feedback switch  $S_f$  and the common-mode ground switch  $S_g$  conduct, resulting in gain of 2 or 4, depending on the stage. The nominal nonunity gain of the stage is simply  $(1 + C_S/C_F)$ . Thus, a gain of two is obtained if  $C_F = C_S$ , while  $C_F = C_S/3$  results in a gain of four. In the first two stages,  $C_F$  is one-third  $C_S$ , while in the third stage  $C_F = C_S$ .

The principle differences between a stage in the VGA and a stage in the pipelined ADC are that no A/D conversion, D/A

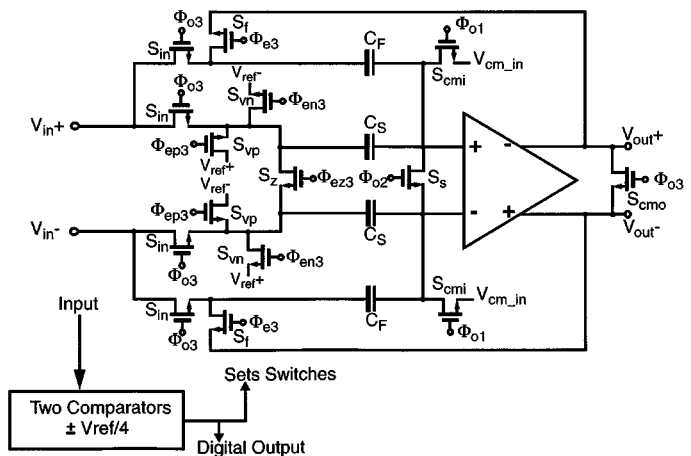


Fig. 5. Schematic of a pipeline A/D converter stage.

conversion, or subtraction are needed in the VGA stage, while there is no unity-gain transfer mode in the ADC pipeline stage, only a gain of two.

### B. Pipelined A/D Converter Stage

The input–output relation for a pipelined A/D converter stage can be expressed as

$$V_{\text{out}} = G(V_{\text{in}} - V_{\text{DAC}}) \quad (2)$$

where  $V_{\text{DAC}}$  is the output of the stage’s D/A converter, and  $G$  is the stage gain of 2 determined by the ratios of sampling capacitors,  $(1 + C_S/C_F)$ . The pipelined A/D converter utilizes digital error correction, which allows lower comparator resolution and correspondingly reduced comparator power dissipation.

As in the VGA stages, each pipelined A/D converter stage has a tracking phase and an amplify/hold phase. The pipelined A/D converter stage, shown in Fig. 5, operates in the same fashion as the VGA stage during the tracking phase. During the amplify/hold phase, capacitor  $C_F$  is connected to the opamp output, and the capacitor  $C_S$  is connected to one of the three designated reference voltages  $\{-V_{\text{ref}}, 0, +V_{\text{ref}}\}$ . The 2-b A/D conversion provided by the comparators in the stage governs the operation of the switches  $S_{vp}$ ,  $S_{vn}$ , and  $S_z$  during the amplify/hold phase and determines the reference to which  $C_S$  is connected. If the input voltage is greater (less) than  $+V_{\text{ref}}/4$  ( $-V_{\text{ref}}/4$ ), then  $S_{vp}$  ( $S_{vn}$ ) turns on to connect  $C_S$  to  $+V_{\text{ref}}$  ( $-V_{\text{ref}}$ ). If the input voltage is between  $+V_{\text{ref}}/4$  and  $-V_{\text{ref}}/4$ , then  $S_z$  connects  $C_S$  to a common-mode ground. During the amplify/hold phase the residue of the stage is amplified and acquired by the following stage in the pipeline.

Since digital error correction is used to correct for the potentially large offsets in these circuits, simple low-power dynamic comparators are used in the pipelined A/D converter, as in [1]. The comparators act as a low-resolution flash A/D converter that adds little capacitance to the load on the preceding stage.

### C. Operational Amplifiers

The opamps used in each stage of the FADC employ a telescopic cascode structure with gain-booster cascode devices [6], [7]. Capacitive common-mode feedback generates the current source bias voltage. The common-mode input and output levels

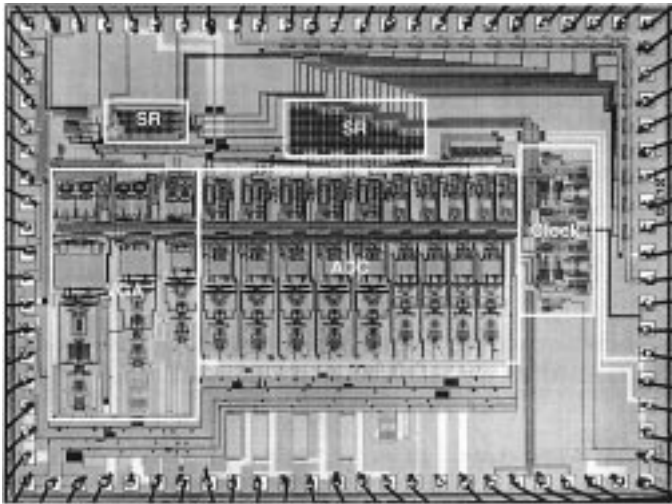


Fig. 6. Die photo.

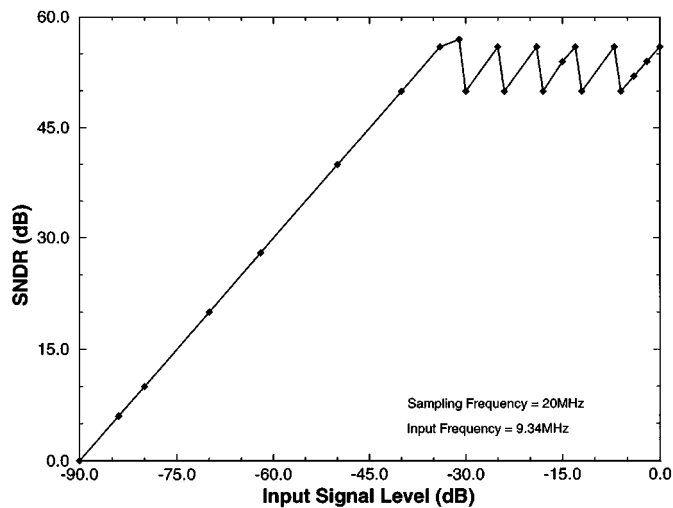


Fig. 7. Plot of the SNDR ratio of the experimental FADC as a function of the input signal level at 9.34 MHz.

for both the main opamp and the gain boosting amplifiers are established during the tracking/sampling phase for each stage. The gain-boosting amplifiers are also telescopic cascode circuits with capacitive common-mode feedback.

#### IV. EXPERIMENTAL RESULTS

An experimental 15-b FADC has been designed and implemented in a 0.5- $\mu\text{m}$  triple-metal CMOS technology with linear poly/n-well capacitors. The static power dissipation was measured at 122 mW for a 5-V analog supply. The digital circuits, including the clock circuitry, shift registers, and comparators, dissipated 258 mW. The clock generator used large inverters to minimize the rise and fall times for precise multiphase clocking throughout the chip. A die photo of the pad-limited design, which has dimensions of 4.3 mm  $\times$  3.2 mm, is shown in Fig. 6. The stages of the VGA were aggressively scaled in proportion to their maximum closed-loop gain, and the stages of the pipeline A/D converter were scaled more gradually.

To minimize offsets and capacitor mismatch, special care was taken in the physical layout of the converter [8]. Precautions

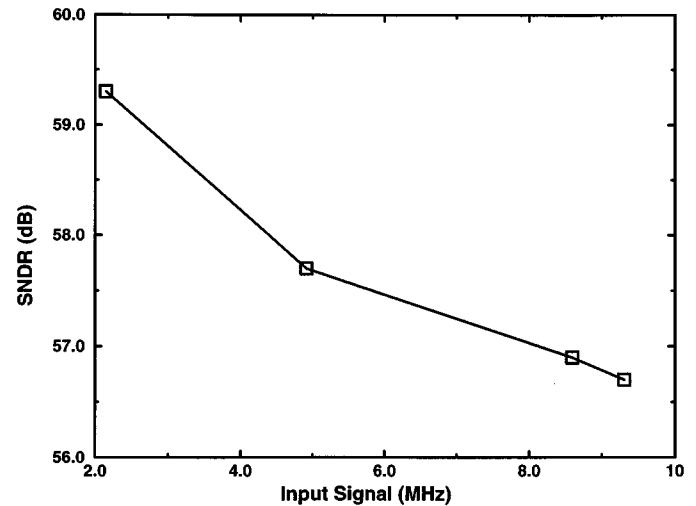


Fig. 8. Peak SNDR versus input signal frequency.

TABLE I  
FADC PERFORMANCE SUMMARY

Parameter	Value
Sampling Rate	20 MSample/sec
Peak SNDR	60 dB
Dynamic Range	90 dB
Supply Voltage	5V analog, 4.5V digital
Power dissipation	380 mW
Technology	0.5- $\mu\text{m}$ triple-metal CMOS with linear Poly/Nwell caps
Active Area	4.3 mm $\times$ 3.2 mm

taken include shielding sensitive signals, common-centroid device placement, mirror symmetry, and separation of the analog and digital circuitry. Separate supplies were used for the clock generator and output drivers, as well as for the analog and digital sections.

A plot of the SNDR measured for the experimental FADC as a function of the input signal level is shown in Fig. 7 for sinusoidal signal at 9.34 MHz, near the Nyquist band edge. As the input signal frequency is reduced, the maximum SNDR increases, as shown in Fig. 8. The peak SNDR for the converter is 59 dB, and the maximum dynamic range is 90 dB for an input sinusoid at 2.1 MHz, sampled at a rate of 20 MSample/s. As the input frequency is increased close to the Nyquist band edge, there is less time for the sensitive signals to settle from switching disturbances in the input sample-and-hold. The measured performance of the experimental FADC is summarized in Table I.

#### V. CONCLUSION

As the complexity and scope of digital information processing increases, analog-to-digital converters are ever more critical links between the analog and digital domains. In some applications, however, not all of the information embedded in the analog signal is needed.

Floating-point A/D conversion enables the digitalization of analog signals with an extended dynamic range. This conversion approach can reduce the need for calibration and high lin-

earity while still achieving a large dynamic range. An experimental prototype has demonstrated the successful operation of a floating point A/D converter with ten bits of resolution and 90 dB of dynamic range at a sampling rate of 20 MSamples/s.

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